METHOD FOR A JUNCTION FIELD EFFECT TRANSISTOR WITH REDUCED GATE CAPACITANCE

FIELD OF THE INVENTION

Embodiments of the present invention relate to field effect transistors (FETs). In particular, embodiments of the present invention relate to a gate structure for improved performance characteristics in FETs.

BACKGROUND ART

Junction field effect transistors (JFETs) are majority carrier devices that conduct current through a channel that is controlled by the application of a voltage to a p-n junction. JFETs may be constructed as p-channel or n-channel and may be operated as enhancement mode devices or depletion mode devices. Similar to the JFET is the metal-semiconductor field effect transistor (MESFET). In MESFETs, a junction between a metal and a semiconductor is used to create a Schottky barrier that takes the place of the p-n junction of the JFET.

The most common JFET type is the depletion mode type. The depletion mode device is a "normally on" device that is turned off by reverse biasing the p-n junction so that pinch-off occurs in the conduction channel. P-channel depletion mode devices are turned off by the application of a positive voltage between the gate and source (positive V_{gs}), whereas n-channel depletion mode devices are turned off by the application of a negative voltage between the gate and source (negative V_{gs}). Since the junction of a depletion mode JFET is reverse biased in normal operation, the input voltage V_{gs} can be relatively high. However, the supply voltage between the drain and source (V_{ds}) is usually relatively low when the device is turned on.

Prior Art FIG. 1 shows a general schematic for an n-channel depletion mode JFET with $V_{gs}=V_{ds}=0$. The JFET has two opposed gate regions 10, a drain 11 and source 12. The drain 11 and source 12 are located in the n-doped region of the device and the gates 10 are p-doped. Two p-n junctions are present in the device, each having an associated depletion region 13. A conductive channel region 14 is shown between the two depletion regions 13 associated with the p-n junctions. In operation, the voltage variable width of the depletion regions 13 is used to control the effective cross-sectional area the of conductive channel region 14. The application of a voltage V_{gs} between the gates 10 and source 12 will cause the conductive channel region to vary in width, thereby controlling the resistance between the drain 11 and the source 12. A reverse bias, (e.g., a negative V_{gs}), will cause the depletion regions to expand, and at a sufficiently negative value cause the conductive channel to "pinch off", thereby turning off the device.

The width of the depletion regions 13 and the conductive channel region 14 are determined by the width of the n-doped region and the dopant levels in the n-doped and p-doped regions. If the device shown in FIG. 1 were constructed with a narrow n-doped region, such that the two depletion regions merged into a single continuous depletion region and the conductive channel region 14 had zero width, the result would be the device shown in Prior Art FIG. 2.

Enhancement mode, or "normally off" JFETs are characterized by a channel that is sufficiently narrow such that a depletion region at zero applied voltage extends across the entire width of the channel. Application of a forward bias reduces the width of the depletion region in the channel,

thereby creating a conduction path in the channel. P-channel enhancement mode JFETs are turned on by the application of a negative V_{gs}, and n-channel enhancement mode JFETs are turned on by the application of a positive V_{gs}. The input gate voltage of an enhancement mode JFET is limited by the forward voltage of the p-n junction.

Prior Art FIG. 2 shows a general schematic of an n-channel enhancement mode JFET with $V_{gs}=V_{ds}=0$. The enhancement mode device is "normally off" since the conductive channel width is zero due to the extent of the two depletion regions 13B. The application of a sufficient forward bias (e.g. positive V_{gs}) to the device of FIG. 2 will cause the depletion regions 13B to contract, thereby opening a conductive channel.

Although the depletion mode and enhancement mode devices shown schematically in FIG. 1 and FIG. 2 are n-channel devices, depletion mode and enhancement mode devices could be constructed with a reversed doping scheme to provide p-channel devices.

JFETs are capable of being driven by low voltages while maintaining excellent breakdown characteristics when compared to MOSFETs. Since there is no insulator associated with gate/drain and gate/source interfaces of a JFET (only a p-n junction), forward bias results in conduction at a voltage that is very low compared to the reverse bias that the device is capable of withstanding. JFETs also have a much greater resistance to damage from electrostatic discharge (ESD) than MOSFETs.

Historically, metal-oxide semiconductor field effect transistors (MOSFETs) have been much more widely used than JFETs, and among JFETs, the depletion mode device has been more widely used than the enhancement mode device. However, the adoption of submicron processes for device fabrication and the resulting higher speeds, lower voltages, and greater current demands in integrated circuits has created new opportunities for the application of JFETs.

As improvements in photolithographic processes has reduced the lateral resolution for device features, the vertical composition of device features (e.g., the gate and its associated p-n junctions) has remained relatively unchanged with respect to processes involving ion implantation and thermal diffusion.

For vertical FET devices, the lack of close control over the device characteristics in the vertical dimension results in longer channel lengths, increased leakage current, and increased parasitic capacitance.

Thus, a need exists for a method that provides improved control over the vertical feature characteristics in JFETs and MESFETs. There is also a need for a gate structure with improved performance characteristics.

SUMMARY OF INVENTION

Accordingly, embodiments of the present invention provide enhanced control over the vertical characteristics of gate structures of JFETs and MESFETs. In embodiments of the present invention, multiple ion implantation steps are used to provide a dual gate structure that reduces the effective channel length, leakage current, and parasitic capacitance in JFETs and MESFETs.

A method for fabricating a dual gate structure for JFET and MESFET devices is disclosed. Trenches are etched in a semiconductor substrate for fabrication of a gate structure for a JFET or MESFET. A sidewall spacer may be formed on the walls of the trenches to adjust the lateral dimension for a first gate. Following the formation of the first gate, a buffer region is implanted below the first gate using a complementary dopant and a second sidewall spacer with a thickness that may